REMARKS

The Office Action mailed on March 13, 2003, has been received and reviewed.

Claims 1-28 are currently pending in the above-referenced application. Each of claims 1-28 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Preliminary Amendment

Please note that a Preliminary Amendment was filed in the above-referenced application on May 17, 2002, but that the Office has not yet acknowledged entry of the Preliminary Amendment. If, for some reason, the Preliminary Amendment has not yet been entered, the undersigned attorney would be happy to provide a true copy thereof to the Office.

Obviousness-Type Double Patenting Rejection

Claims 1-28 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-26 and 28-37 of U.S. Patent 6,372,643. A terminal disclaimer and the appropriate fee are being filed herewith, pursuant to 37 C.F.R. § 1.321(b) and (c), to obviate the obviousness-type double patenting rejection, thereby expediting prosecution of the above-referenced application and avoiding further expense and time delay. The filing of a terminal disclaimer in the above-referenced application should not be construed as acquiescence of the obviousness-type double patenting rejection.

Rejections Under 35 U.S.C. § 103(a)

Each of claims 1-28 has been rejected under 35 U.S.C. § 103(a). M.P.E.P. § 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable

expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Hrzek in View of Levine

Claims 1, 8-13, 15-17, 20, and 23-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 3,801,365 to Hrzek (hereinafter "Hrzek"), in view of U.S. Patent 5,989,999 to Levine et al. (hereinafter "Levine").

Hrzek teaches a process for forming conductive structures, including metal silicide contacts. The process of Hrzek includes introducing a mixture that includes sublimated molybdenum pentachloride, hydrogen, and argon onto the surface of a heated silicon wafer. Col. 6, lines 27-47. When the metal pentachloride contacts the heated silicon, it purportedly gives off elemental chlorine and forms a metal subchloride. Col. 3, lines 45-49. The elemental chloride purportedly reacts with the silicon to form a silicon chloride, which purportedly reacts with the metal subchloride to form the metal (*i.e.,* molybdenum) silicide. Col. 3, lines 49-53.

Although Hrzek refers to this process as a metal silicide "deposition" process, it is clear that the metal silicide is not deposited onto the silicon wafer (*i.e.,* formed above the silicon wafer), but formed as a reaction occurs at the surface of the silicon wafer.

Hrzek is silent as to the subsequent formation of a metal nitride over the metal silicide. Rather, the teachings of Hrzek are limited to forming metal silicide of various types (*e.g.,* $MoSi_2$, then Mo_3Si), then metal (*e.g.,* Mo). Col. 7, lines 45-50.

Levine teaches processes for forming metal nitride barrier layers. The process of Levine includes depositing a metal nitride onto silicon (col. 4, lines 20-29; col. 15, lines 48-51), annealing the metal nitride (col. 4, lines 30-42; col. 15, lines 48-51), then oxidizing (col. 4, lines 43-46; col. 28, lines 42-46) or "stuffing" the metal nitride with silicon atoms (col. 4, lines 46-48; col. 32, lines 52-59). Levine also teaches that all of these processes may be conducted in the same chamber, or *in situ*. Col. 4, lines 49-55.

Levine does not teach that the metal nitride barrier layers thereof may be formed on metal silicide structures, let alone *in situ* with the formation of metal silicide structures.

Independent claim 1 of the above-referenced application recites a method for fabricating an interconnect adjacent a contact of a semiconductor device structure which includes depositing a metal silicide directly onto at least one exposed, doped area of a semiconductor device structure and depositing an interconnect material onto the metal silicide *in situ* with the metal silicide deposition. Independent claim 1 requires that the metal silicide deposition occur without substantially deposition metal silicide onto locations of the semiconductor device structure that are laterally adjacent exposed, doped areas thereof.

Independent claim 20 is drawn to a method for fabricating a selective contact and a local interconnect. The method of independent claim 20 includes depositing a contact material directly onto an exposed active device region of a semiconductor device structure without substantially depositing contact material onto locations of the semiconductor device structure that are laterally adjacent the exposed active device region, then, *in situ,* depositing an interconnect material onto the contact material.

It is respectfully submitted that a *prima facie* case of obviousness has not been established against either independent claim 1 or independent claim 20 for several reasons.

First, it is respectfully submitted that Hrzek and Levine, taken either separately or in combination, do not teach or suggest each and every element of either independent claim 1 or independent claim 20. Specifically, neither Hrzek nor Levine teaches or suggests "depositing metal silicide directly *onto* at least one exposed, doped area of a semiconductor device structure . . ." (emphasis supplied), as recited in independent claim 1, or "depositing a contact material directly *onto* an exposed active device region of [a] semiconductor device structure . . ." (emphasis supplied), as recited in independent claim 20. More specifically, the teachings of Hrzek are limited to a process that includes reacting silicon atoms at a surface of a semiconductor substrate (*i.e.,* a silicon wafer) with other reactants to form metal silicide (*i.e.,* molybdenum silicide) *at* that surface. As the metal silicide of Hrzek is formed by consuming atoms at the surface, it is clear that the metal silicide is not deposited *onto* that surface.

Levine is altogether devoid of any teaching or suggestion regarding the deposition of metal silicides.

Moreover, both references lack any teaching or suggest that another deposition process may be conducted *in situ* with the particular material formation process taught therein (*i.e.,* metal silicide in Hrzek; metal nitride in Levine).

Second, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Hrzek and Levine in the manner that has been asserted. Again, Hrzek lacks any teaching or suggestion of the deposition of a metal nitride layer over the metal silicide structure formed therein. Instead, the teachings of Hrzek are limited to the deposition of metal (*e.g.,* molybdenum) directly onto metal silicide (*e.g.,* Mo_3Si). Col. 7, lines 45-50. Thereafter, a layer 80 (FIG. 3) of semiconductor memory material, which is a material that, in a first state has high electrical resistance and in a second state has low electrical resistance (*see,* U.S. Patents 3,271,591 and 3,530,441, both of which are cited and incorporated by reference into Hrzek), not a metal nitride, may be formed over the metal silicide structure. Levine likewise lacks any teaching or suggestion that the metal nitride layer thereof may be deposited onto a metal silicide structure. In fact, Levine, at col. 3, lines 5-23, provides context for the metal nitride layer deposition and annealing processes described therein: the metal nitride layer is to be formed so as to contact a conductive region 105 of a silicon substrate 101. Col. 3, lines 5-7. As neither of these references teaches that a metal silicide layer and a metal nitride layer could be used in conjunction with one another, it is respectfully submitted that these references would not have provided one or ordinary skill in the art with any motivation to combine their teachings.

Rather, due to the fact that there is not motivation or suggestion in these references that would provide one of ordinary skill in the art with some motivation or suggestion to link their teachings, it appears that the only source for such motivation could have been the teachings of the above-referenced application. Therefore, it is respectfully submitted that the asserted combination of Hrzek and Levine could only have been based on improper hindsight provided by the teachings of the above-referenced application.

Third, it is respectfully submitted that one of ordinary skill in the art would have had no reason to expect the asserted combination of Hrzek and Levine to be successful. In particular, when the teachings of Hrzek and Levine are considered in their entireties, as required by

M.P.E.P. § 2141.02, it is clear that there would be no way to intersperse the process of Levine in between the metal silicide deposition and metal deposition portions of the process of Hrzek.

In view of the foregoing, it is respectfully submitted that Hrzek and Levine do not support a prima facie case of obviousness against either independent claim 1 or independent claim 20.

Claims 8-13 and 15-17 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Each of claims 23-28 is allowable, among other reasons, as depending either directly or indirectly from claim 20, which is allowable.

Claims 11 and 24 are further allowable since Hrzek and Levine both lack any teaching or suggestion of depositing an interconnect material *selectively* onto a metal silicide (claim 11) or contact material (claim 24).

It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), each of claims 1, 8-13, 15-17, 20, and 23-28 is allowable over the asserted combination of Hrzek and Levine.

Hrzek in View of Levine and Chang

Claims 2-5, 21, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hrzek, in view of Levine and, further, in view of U.S. Patent 5,043,299 to Chang et al. (hereinafter "Chang").

Claims 2-5 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claims 21 and 22 are both allowable, among other reasons, as respectively depending directly and indirectly from claim 1, which is allowable.

Moreover, Chang, which is directed to a process for selectively depositing tungsten onto unmasked areas of a masked semiconductor device structure and which is relied upon for its teaching that a semiconductor device structure may be exposed to a plasma for the purpose of cleaning, does not include any teaching or suggestion which would remedy the lack of motivation

in Hrzek and Levine.

Nor does Chang provide any teaching or suggestion which would provide one of ordinary skill in the art with some reason to expect that the asserted combination of Hrzek and Levine would be successful.

Hrzek in View of Levine and Kolar

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hrzek, in view of Levine and, further, in view of U.S. Patent 5,162,259 to Kolar et al. (hereinafter "Kolar").

Claims 6 and 7 are both allowable, among other reasons, as respectively depending directly and indirectly from claim 1, which is allowable.

Kolar teaches a process for forming a buried, self-aligned metal silicide contact, as well as the formation of a metal interconnect in contact therewith. Kolar is relied upon for its teaching that the semiconductor device structure on which the metal silicide contact is formed may be cleaned following the formation of the metal silicide contact. Kolar does not, however, remedy the motivational deficiency of Hrzek and Levine. Nor does Kolar provide one of ordinary skill in the art with any reason to believe that the asserted combination of Hrzek and Levine would be successful.

Hrzek in View of Levine and Park

Claims 14, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hrzek, in view of Levine and, further, in view of U.S. Patent 6,087,257 to Park et al. (hereinafter "Park").

Each of claims 14, 18, and 19 is allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Moreover, Park, which is relied upon for its teaching of processes for forming tungsten nitride interconnects, does not remedy the aforementioned deficiencies of Hrzek and Levine. In particular, the teachings of Park are limited to the formation of interconnects directly on an active device region. Thus, Park does not provide any motivation to one of ordinary skill in the art to

form a metal silicide onto the active device region prior to forming a metal nitride interconnect thereover, let alone that a metal silicide or other contact material may be deposited *in situ* with an interconnect material.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-28 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 1-28 is allowable. An early notice of the allowability of each of these claims, as well as an indication that the above-referenced application has been passed for issuance, are respectfully solicited. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

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